

5. The computer as claimed in claim 1,
wherein said data holding part holds an instruction
address of an instruction which causes said
interrupt.

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6. The computer as claimed in claim 1,
10 wherein said data holding part holds data which
indicates a factor of said interrupt.

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7. The computer as claimed in claim 1,
wherein said data holding part holds an effective
address of a load instruction or a store instruction
when said interrupt occurs while said load
20 instruction or said store instruction is executed.

8. The computer as claimed in claim 1,
25 wherein said data is used for recovery from said
interrupt.

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9. A control method of a computer which
processes an interrupt when an instruction in a
program is executed, said method comprising the step
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holding data at a time when said interrupt
starts to occur.

5 10. The control method as claimed in claim
9, wherein said data is held in a plurality of
registers and said data is used for recovery from a
plurality of interrupts.

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11. The control method as claimed in claim
10, wherein flags are used in which each of which
15 flags indicates whether said data is held in said
register.

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12. The control method as claimed in claim
9, said control method comprising the step of:
holding said data to be stored in a data
storing part in said computer at a time when said
25 interrupt occurs while a store instruction is
executed, said store instruction requesting that
said data is stored in said data storing part.

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13. The control method as claimed in claim
9, said control method comprising the step of:
holding an instruction address of an
35 instruction which causes said interrupt.

5 holding data which indicates a factor of
said interrupt.

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